Electro-migration Reliability Verification of Gate Level Blocks for High Performance Microprocessors in Presence of Self-Heating

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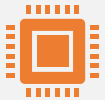
Motivation



EM reliability verification is a key challenge in the design of a microprocessor in 14 nm technology.

Increasing interconnect current densities, higher current drive of FINFETs, a multi-billion transistor chip, and elevated temperatures due to local self-heating all required us to look for a robust EM verification methodology.

Since large parts of the design were implemented out of library cells, we needed to devise an efficient method of verifying each cell’s EM reliability

Background

Current in the interconnect is a function of voltage, frequency, capacitance on outputs, and transition time (slew) of inputs.

Current limit of the interconnect is a function of layout (interconnect length, width and metal level), temperature and power-on-hours (POH).

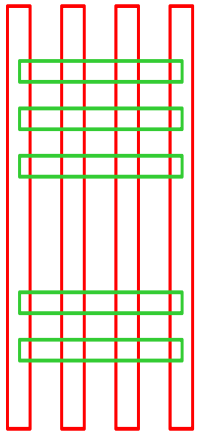
Self-heating in cells depends on power and thermal resistance (RTH), the latter a function of the layout.

Main Idea

Characterization of standard cells in the library for Rth, Max Slew and Max Cap.

Validation of cell instances for EM during either the block construction or sign-off phase.

Characterization Phase Details -- RTH.



2 finger, 3 FIN pfet, RTH_p

2 finger, 2 FIN nfet, RTH_n

RTHcell=1.3*(RTH_n*RTH_p)/(RTH_n+RTH_p)

Transistor models in the Process Design Kit (PDK) provide RTH values for isolated FETs as a function of the number of fingers and FINs.

Using this information and accounting for NFET-PFET proximity in the layout, we computed a RTH value for each library cell.

Knowing a cell's RTH and the power for each instance, allowed us to compute Delta T, the temperature rise due to self-heating, where DT=RTH*Power.

Characterization Phase Details – Max Slew

Frequency in GHz

Voltage in Volts	0.1	0.3	0.6	1.3	2.6	5.2	8.0
0.6	1e-9						
0.7							
0.8							
0.9							
1.0							
1.1							
1.2							-1

Each Entry Indicates Maximum Allowed Input Slew

A set of MAX_SLEW tables at different Temp/POH points were generated for each cell.

Each table has Voltage and Frequency as independent variables. Each entry in MAX_SLEW table contains maximum allowed slew on the input that satisfies EM requirements.

One set of MAX_SLEW tables were generated for multi-input cells.

Each entry for a Voltage, Frequency combination generated through circuit simulations (all output capacitances set to zero). each combination checked to ensure IRMS and IPeak satisfy EM requirements

To determine EM requirements failure point, multiple simulation iterations done with increasing input slew until the failure point is observed,

MAX_SLEW tables assure EM robustness in most of the interconnect of the cell, except for that of the outputs.

Characterization Phase Details – Max Cap

Input Slew in ps

Voltage in Volts	4	20	40	80	160	400	2K
0.6	1e12						
0.7							
0.8							
0.9							
1.0							
1.1							
1.2							-1

Each Entry Indicates Maximum Allowed Output Capacitance

A set of MAX_CAP tables at different Temp/POH points were generated for each output port of every cell.

While each table could have F, V and Slew as independent variables to model single stage cells. We limit MAX_CAP tables to Voltage, Slew only, while fixing Frequency to 25 MHz.

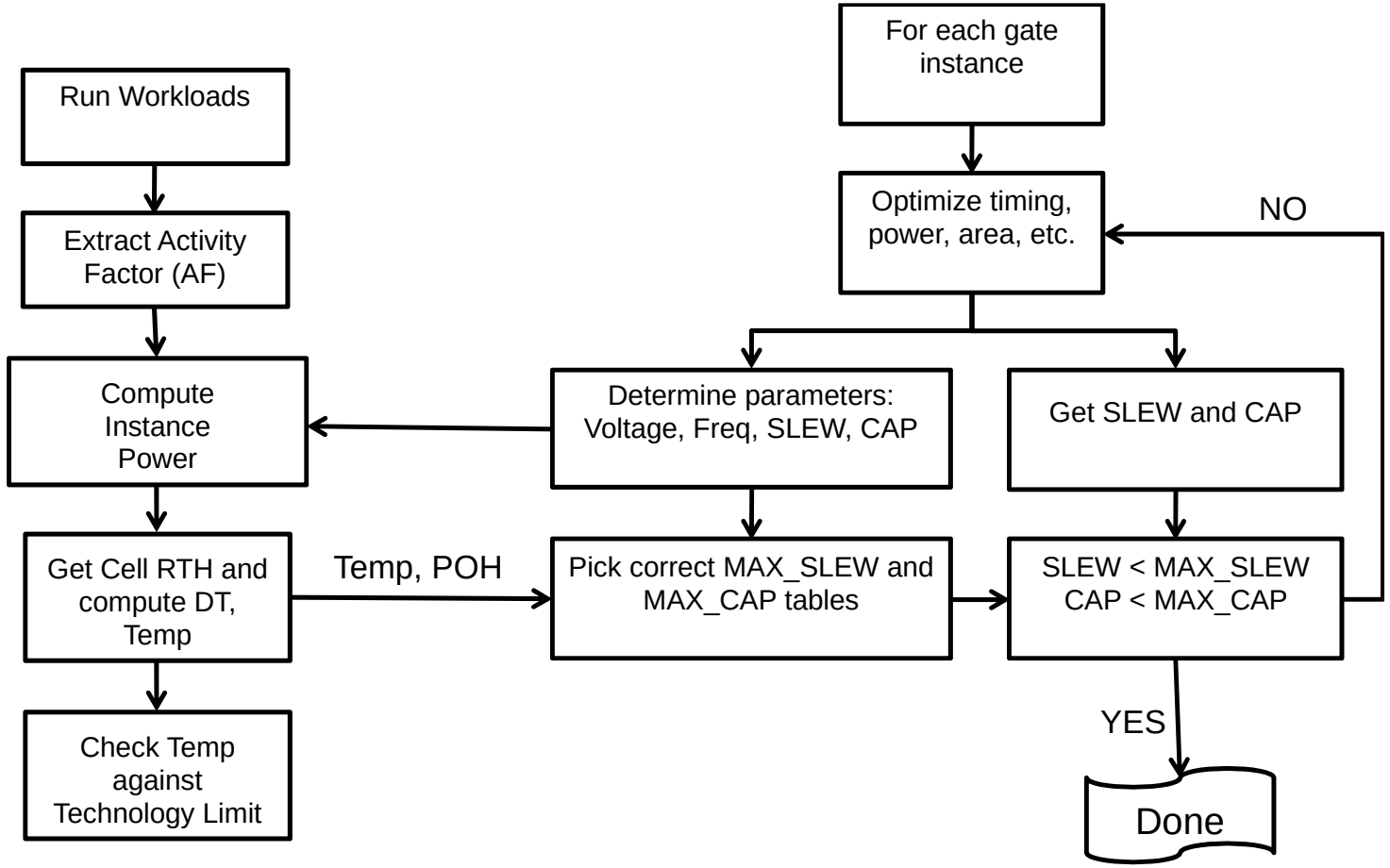
Values are scaled to actual Frequency used. Each entry contains maximum allowed capacitance on the output that just satisfies EM requirements.

Larger capacitances create currents that violate the requirements.

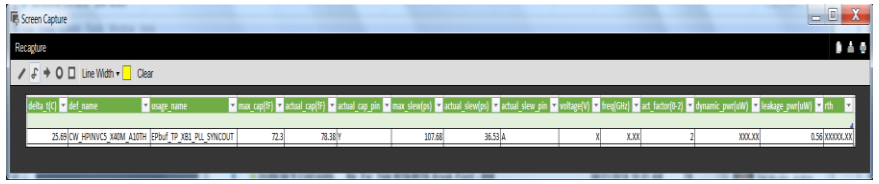
During characterization, only interconnect associated with specific output port is checked, EM failure point is derived from simulations similar to those for MAX_SLEW.

MAX_CAP tables ensure EM robustness in all the output interconnect of the cell.

Main Idea – Validation Phase Details



Experimental Results



unit	# cells	# DT fails	# MAX_CAP fails	# MAX_SLEW fails
DESIGN1	2489066	19	87	3
DESIGN2	309373	7	10	0
DESIGN3	4579	0	5	0
DESIGN4	2149	0	0	0
DESIGN5	369	0	0	0
DESIGN6	12000	0	0	0
DESIGN7	43593	0	0	0
DESIGN8	17463	0	0	0
DESIGN9	30569	0	0	0

- Example report at the sign-off phase listing a cell instance in violation of the MAX_CAP limit, as well as violation statistics for a subset of blocks.
- Left over violations were fixed manually. MAX_CAP and MAX_SLEW violations were fixed via known techniques.
- High DT violations were fixed by either reducing instance power by lowering load capacitance, or increasing the instance power level.

Conclusion

we used a two-step method of library cell characterization and correct-by-construction (or sign-off) validation to check EM compliance of cell-based blocks in the presence of self-heating.

This method was successfully used to verify an EM design of multi billion transistor, 5+ GHz microprocessor.